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Design and Implementation of Full Adder Using Vhdl and Its Verification in Analog Domain

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ABSTRACT *: This paper describes the design and implementation of Full adder using VHDL results include successful compilation of VHDL code in Quartus II ,waveforms shows verification of truth table , the result are Also verified in analog domain using analog simulation it also show layout level implementation of full adder using microwind tool, it also shows technological view of full adder along with chip floor plan.*

Keywords – *Full adder ,VHDL, Analog ,Layout ,Chip floor plan*

I. INTRODUCTION

The term digital system include the various system from low level component to complete system over a chip and board –level design .considering a digital system and its complexity it is not possible to understand such a complex system completely, so to make design of a system less complex and understandable VHDL is used .This paper describes the implementation of full adder using VHDL technology which meets less complexity requirement ,it also shows how efficiently digital system ie Full Adder is implemented upto layout level results shows technological map ,RTL view ,chip floor plan ,chip layout ,output waveforms showing voltage Vs time relations and verification of truth table . Following text is divided into three sections; section II describes Full Adder design section III gives simulation results, section IV presents the conclusion.

II. FULL ADDER DESIGN

Full adder is a combinational circuit that has a ability to add two bits and a carry input and produces sum bit and carry bit as output .full adder adds two bits A and B and carry from previous column called as carry input. fig (1) shows logic diagram of full adder table (1)shows truth table of full adder
Fig (2) shows block diagram of full adder.

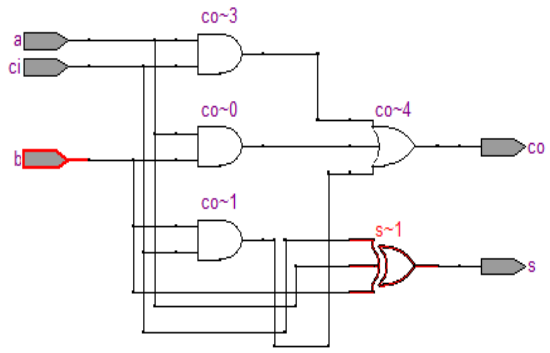
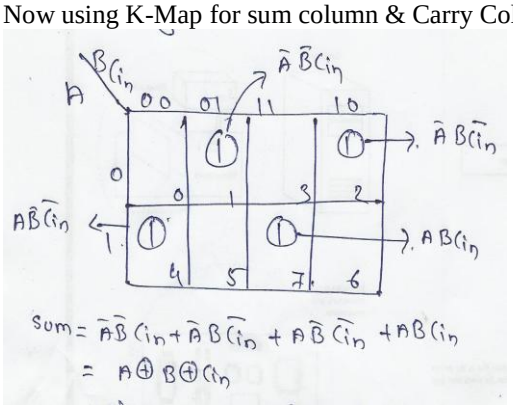


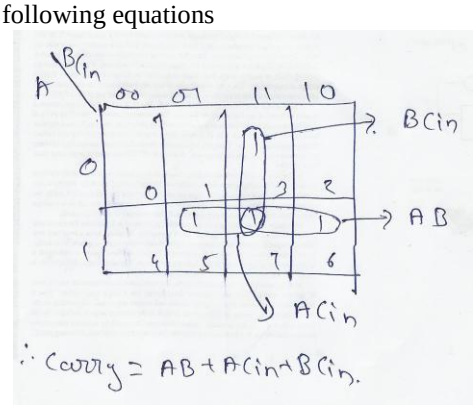
Fig.1: Logic diagram of Full Adder

Table (1): Truth table of full Adder

Inputs			**Sum**	**Carry**
A	B	C	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

From the truth table, a circuit will produce the correct sum and carry bits in response to every possible combination of **A, B**, Cin.
Now using K-Map for sum column & Carry Column we get the following equations





III. SIMULATION RESULTS

All simulation for this full adder has been performed using Quartus II And Microwind tool .A fully integrated Full Adder has been designed,fig (2) shows VHDL code compilation of Full Adder with zero errors and zero warnings .fig(3)shows output waveform of Full adder which verifies the truth table ..fig (4)shows Technological map view .fig(5)shows layout of full adder .fig(6) shows schematic of full adder in analog domain.

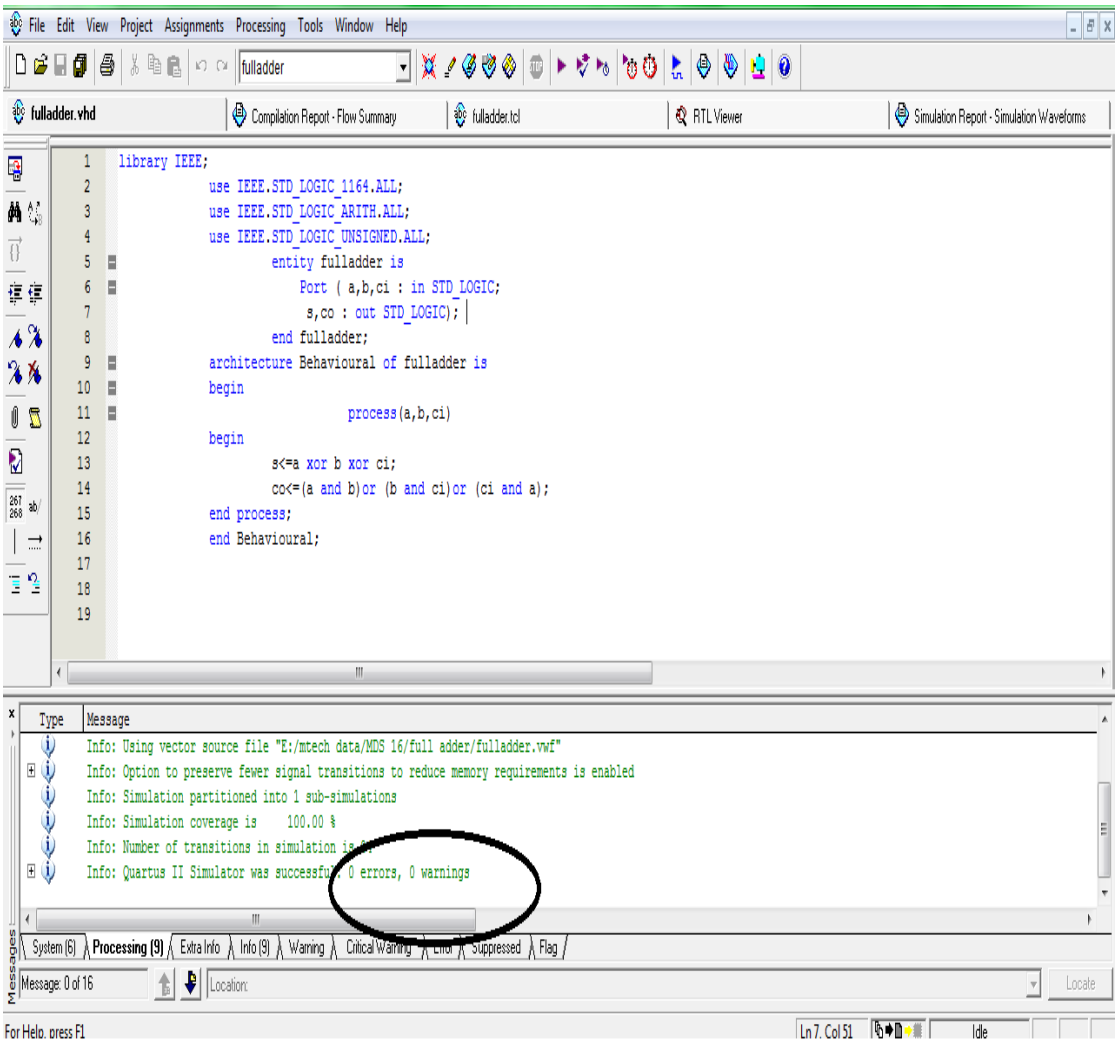


Fig 1: VHDL Code complilation

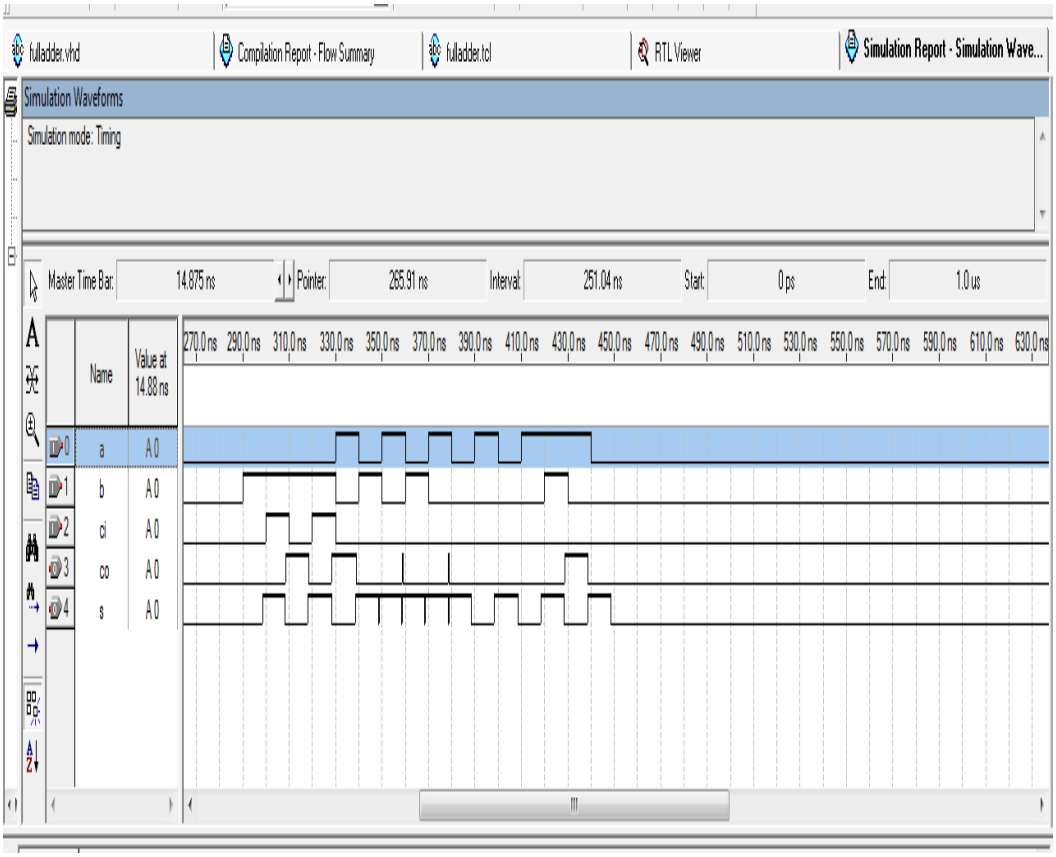


Fig2: output waveform

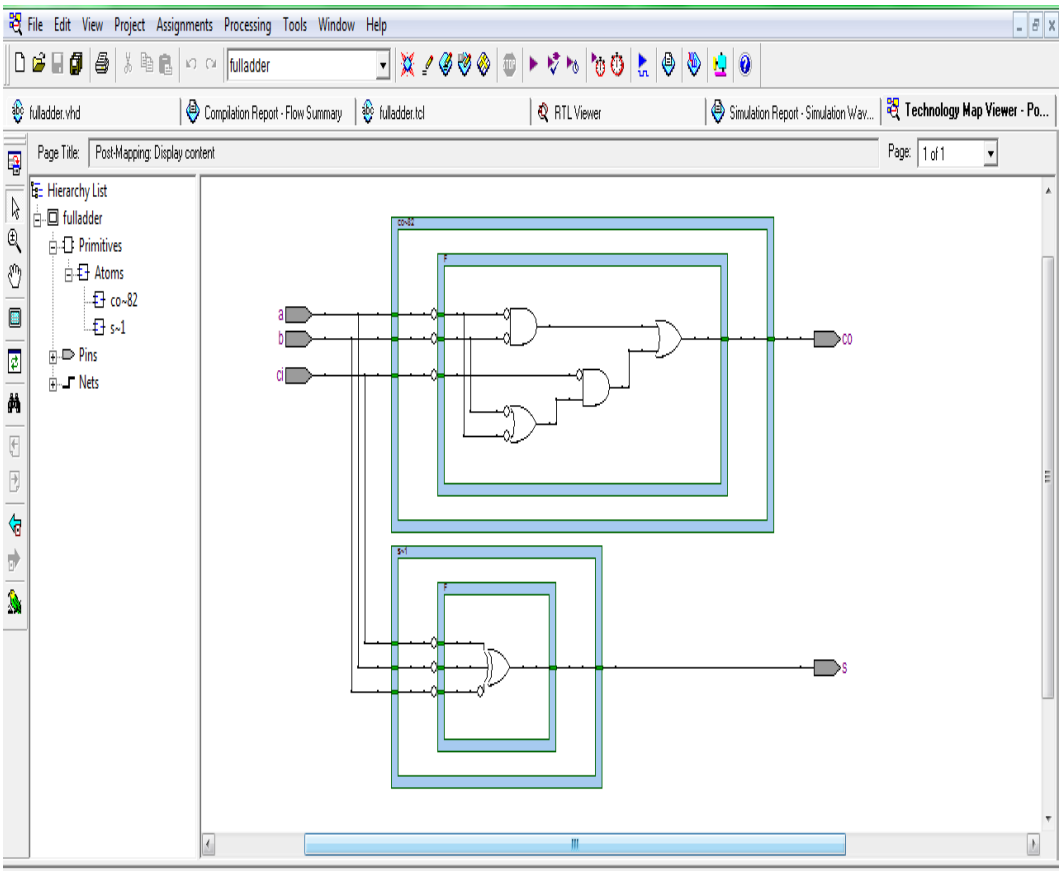


Fig 3: Technological map view

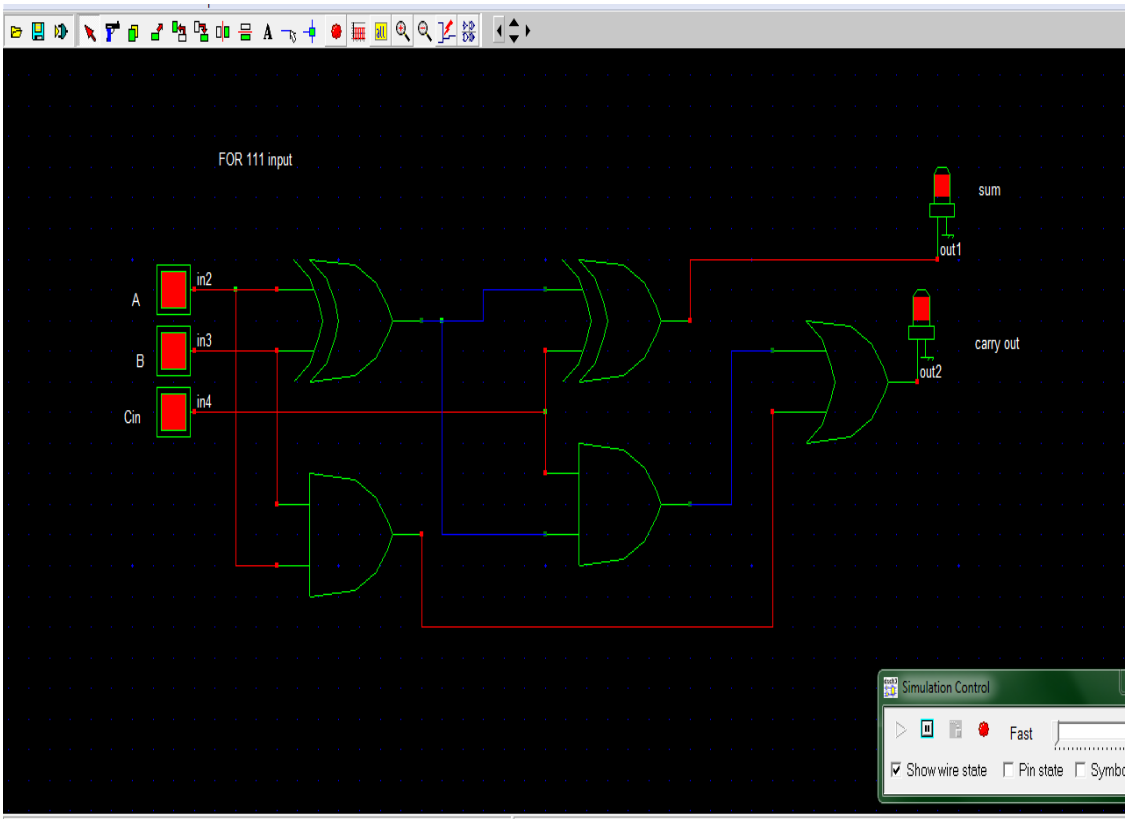


Fig 4: Schematic of full adder in analog domain

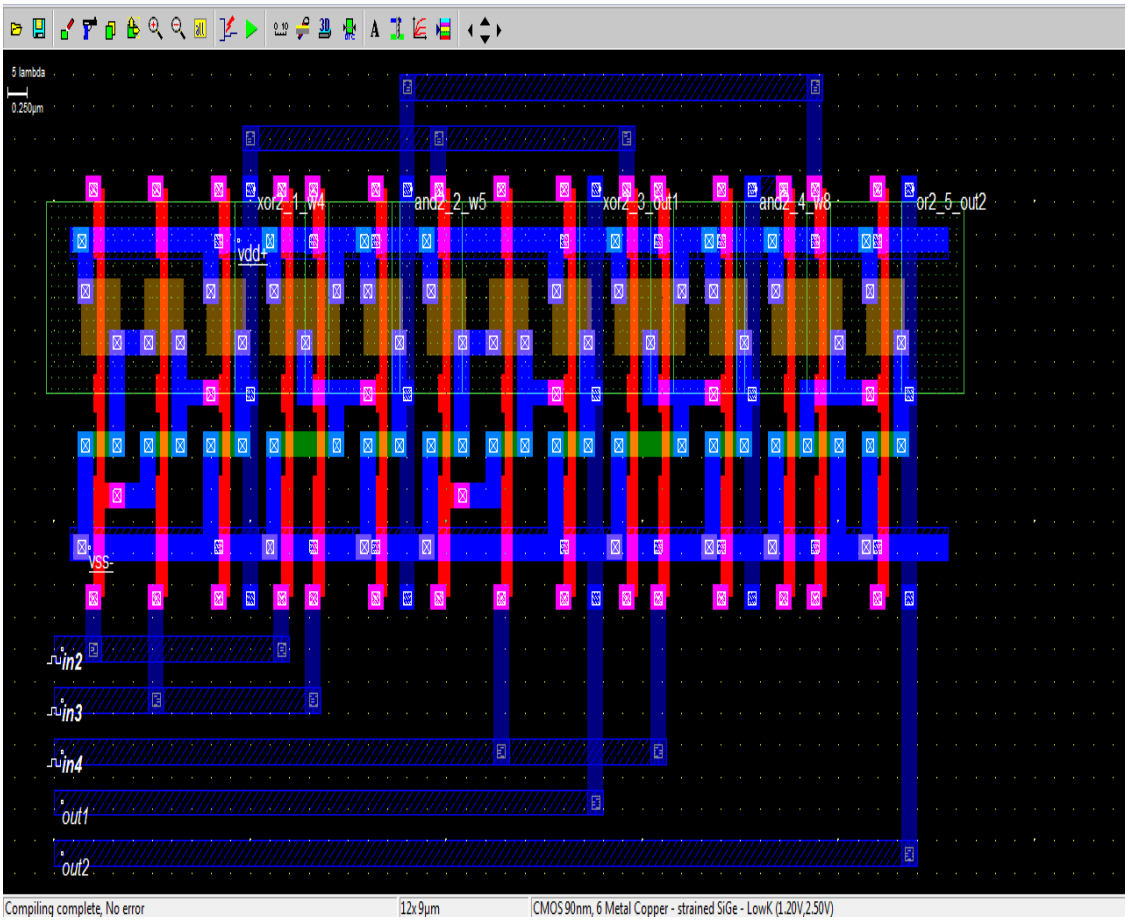


Fig 5: Layout of full Adder circuit

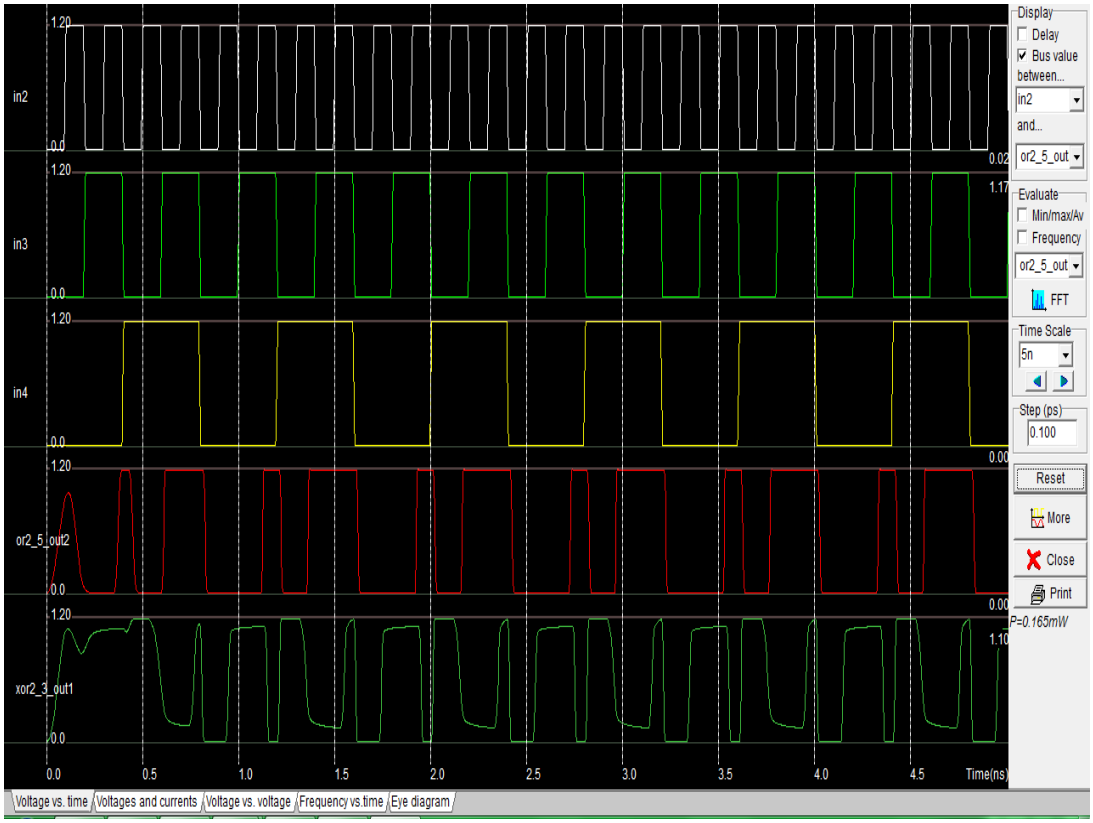


Fig 6: Voltage VS Time relationship in analog domain.

IV. CONCLUSION

CMOS 90nm model is used to design a layout of full adder. Simulation results shows successful compilations of VHDL code and its conversion into verilog file which is used to make a layout using microwind tool.tools used are Quaruts II ,Dsch& microwind . From both performance standpoint and cost standpoint, these results show that CMOS is very competitive with available technologies.

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